Formal models of ARM processors in HOL

More details at: **http://www.cl.cam.ac.uk/~acjf3/arm/**

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- Today's talk
  - very quick overview of ARM and HOL
  - some technical highlights and research challenges
  - making the ARM HOL models accessible (demo)

- General goals of the ARM-in-HOL project
  - accurately model a modern COTS processor
  - use processor model as basis for formal code verification
  - study difficult modelling challenges

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ARM processors and ARM-powered products

- Qualcomm Snapdragon
  - 1GHz design based on ARM Cortex-A8
  - Dell Mini 5 slate, Lenovo Skylight, Google Nexus One
- Texas Instruments OMAP3430
  - 550MHz design based on ARM Cortex-A8
  - Motorola Droid, Nokia N900, Palm Pre
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  - Asus Eee Pad, Notion Ink, Viewsonic, T-Mobile phone
- Marvell Armada 610
  - 1.2GHz based on ARM Cortex-A8, but shorter pipeline
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15 Billion processors created; 10 million shipped every day

[From: `http://www.arm.com/markets/showcase/`]

Higher order logic and the HOL4 system

- Higher order logic intended to formalise mathematics
  - very expressive – can represent all mathematics
  - undecidable – decision procedures for fragments
- HOL4 used in the ARM formalisation project
  - accident of history - could have used other systems
  - Isabelle/HOL, HOL Light, ProofPower use similar logics
- ARM model in first order logic?
  - a challenging case study for the ACL2-HOL link
  - ARM VFP modeled by Reynolds in HOL and ACL2

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Why create formal models of ARM?

- Ultimate goal:
  - high confidence verification of real ARM code
- Need accurate specification of instruction execution
  - ARM supplies 2000 page document in English
- ARM ISA formalised in higher order logic
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Challenges

- How can one be sure the model is correct
  - ARM documentation is voluminous and informal
- IP problems with ARM
  - microarchitectures, tests not easily available to academics
- Several versions of ARM instruction set architecture
  - ARM7 in old phones, Cortex-A8 in smartphones, tablets
- Many modelling research challenges
  - *e.g.* no standard specification of weak memory behaviour

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How can we be sure the model is accurate?

- First approach: prove ISA and hardware models consistent
  - proved ARMv3 ISA consistent with ARM6 machine
  - ARM6 used in Apple Newton
  - modern microarchitectures not available to us
  - Cortex-A8 proof estimated 10x ARMv3 effort

- Second approach: validate by testing against hardware
  - compare deduction in model with execution on ARM

Board	Core
Olimex LPC-2129P	ARM7TDMI-S
Atmel SAM3U-EK	ARM Cortex-M3
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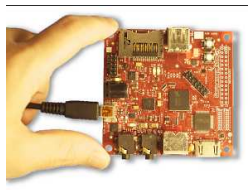

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Single-step theorems

- Single-step theorems derived by instantiating ARM model
  - describe execution of a single instruction
  - derived from ISA-specific configuration
- Executing models for testing
  - single-step theorems generated on-the-fly in HOL4
  - execute by deduction or translation to ML
- Deriving Hoare triples for code verification
  - Hoare triples derived from single-step theorems
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Formal verification of ARM code (Myreen)

- Semantic basis is derived Hoare logic for machine code
  - *e.g.* `E0834004` adds `r3` to `r4` – derived Hoare triple is:

$$\{\ \text{r3}\ a * \text{r4}\ b * \text{pc}\ p\ \}$$
$$p : \texttt{E0834004}$$
$$\{\ \text{r3}\ a * \text{r4}\ (a + b) * \text{pc}\ (p + 4)\ \}$$

- A decompiler extracts functional descriptions from code
  - code below calculates length of a list

```
 0: E3A00000      mov r0, #0          ; set reg 0 to 0
 4: E3510000   L: cmp r1, #0          ; compare reg 1 with 0
 8: 12800001      addne r0, r0, #1    ; if not equal: add 1 to reg 1
12: 15911000      ldrne r1, [r1]      ; load mem[reg 1] into reg 1
16: 1AFFFFFB      bne L               ; jump to compare
```

  - automatically decompiles to function definitions in HOL

$$\text{f}(r_0, r_1, m) = \text{let}\ r_0 = 0\ \text{in}\ \text{g}(r_0, r_1, m)$$

$$\text{g}(r_0, r_1, m) = \text{if}\ r_1 = 0\ \text{then}\ (r_0, r_1, m)\ \text{else let}\ r_0 = r_0{+}1\ \text{in let}\ r_1 = m(r_1)\ \text{in}\ \text{g}(r_0, r_1, m)$$

- Automatically derive a Hoare triple from decompiled code:

$$\{\ (\text{r0}, \text{r1}, \text{m})\ \text{is}\ (r_0, r_1, m) * \text{s} * \text{pc}\ p * \langle \text{f}_{\text{pre}}(r_0, r_1, m) \rangle\ \}$$
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- From

  $$\mathsf{f}(r_1) \quad = \quad \text{if } r_1 < 10 \text{ then } r_1 \text{ else let } r_1 = r_1 - 10 \text{ in } \mathsf{f}(r_1)$$

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Code verification: achievements and goals

- Tiny Lisp interpreter (Myreen)
  - runs on bare metal
  - verified against an independent Lisp language semantics
  - verified garbage collector; tail-call optimisation
  - large word arithmetic for crypto applications (in progress)
  - IO handled by host platform (see Nintendo DS demo)
- Current activity
  - better treatment of IO and exceptions (with John Regehr)
  - realistic multi-core memory (with Peter Sewell)
- Long term goal
  - completely verified useful FP system
  - more work than we can do ... collaborators welcomed!
  - want examples of need for verified FP implementations
- Related non-ARM work at Cambridge
  - Lisp interpreter also runs on x86 and PowerPC models
  - x86 and PowerPC models less complete than ARM
  - Broadcom FirePath processor code equivalence via SMT
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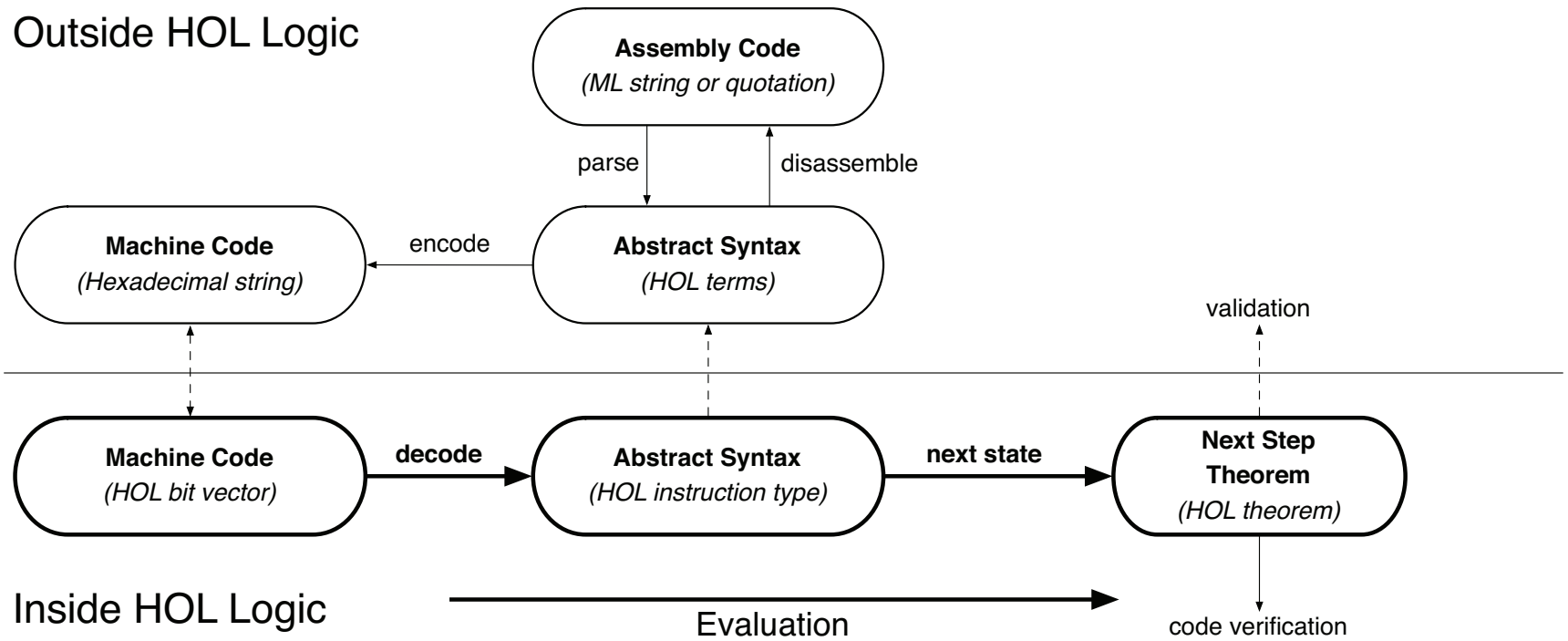
Switch to Anthony ...

Background to current ARMv7 model

- Work on ARMv7 model started towards the end of 2008.
- **Monadic model** — initially requested by Peter Sewell's group (Cambridge).
- Suited to their work on formalizing weak memory models.
  - Cortex-A9 has **multi-core** configurations with **shared memory**.
  - Can reason about the order of register and memory accesses.
- Now used by Magnus Myreen for his code verification work.

Formalization

- Around 24 thousand lines of Standard ML and HOL code. Just under half is HOL definitions and proofs. Only critical parts reside in HOL logic.



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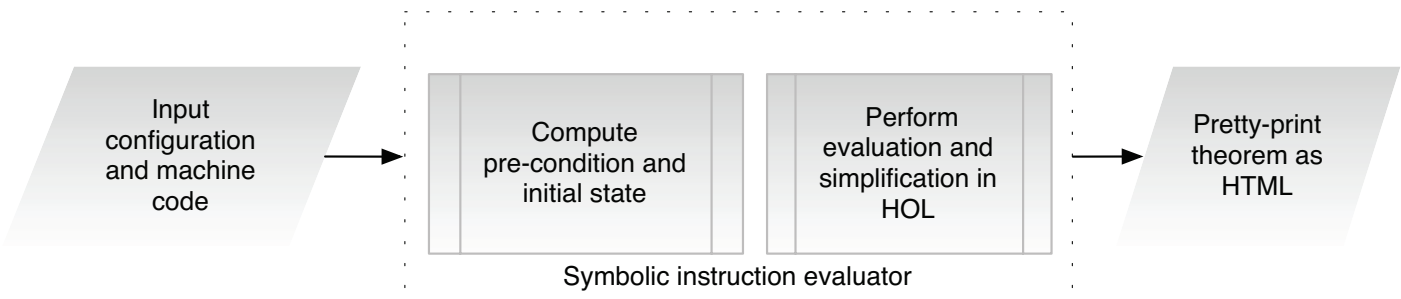
Web Interface (demo)

- A web interface has been built on top of the instruction evaluator.
- **User friendly** input and output. **Hides complexity** of model.
- Easy way to query the model — avoids trawling through the HOL specification.
- Encourage students and formal methods community to use the model.
- Based on CGI scripting: a HOL4 session generates HTML output.



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Summary

- **Large** HOL specification — all standard **ARMv7** instructions covered.
- **Validated** against ARM development boards.
- Instruction evaluator and web interface provides **easy access to the model**.
- Has many uses:
  - Formalizing **shared memory models**.
  - Hardware, system code and compiler **verification**.
- Further collaborations welcomed.
- **Questions?**

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